Q.4 (a) Discuss about ECL and low voltage swing pads. Is there any differences. Give reasons.

(b) Define "setup time" and "hold time" with respect to a CMOS D register. If a clock is delayed to a register with regard to the data input which of these parameters varies and how?

Q.5 (a) Draw and explain the logic structures. Explain with the help of suitable example.

(b) Discuss the mechanism of power dissipation. Write down its classification and explain them in brief.

Q.6 (a) Discuss the design process which elaborates its capture, simulation and verification of any logic structure.

(b) Identify some of the memory and control strategies for subsystem design operations. Write an example.

Q.7 (a) Explain the effective implementation of PLA on CMOS subsystem design operations.

(b) Explain the logic of design abstraction and circuit validation of CMOS circuits.

Q.8 Write short notes on any two of the following:

(a) CMOS Process Enhancements

(b) Non ideal conditions in MOS device model

(c) Various MOSFET Capacitances and their significance

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[Total No. of Questions: 8] *[Total No. of Printed Pages :2]*

Enroll No…….

EC-101

M.Tech. (DC)–I Sem (Reg./Ex.) Examination, March-2021

VLSI Design

Time: Three Hours

Maximum Marks:70

Note: Attempt any five questions. (Each question carries equal marks)

Q.1 (a) Write an introductory note on fundamental design of digital CMOS circuits.

(b) Explain the concept of integrated circuits and its manufacturing technologies. Explain any one technology in detail with the help of suitable example.

Q.2 Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.

Q.3 Realized the Boolean expression Z = (D'.F'.A') + (B'.C')F' using standard CMOS and also find the equivalent CMOS inverter circuit assuming that (W/L)p = 10 for all PMOS transistors and (W/L)p = 5 for all NMOS transistors.